WHAT IS CLAIMED IS:

1. A method of forming an electrically conductive element in an integrated circuit, the method comprising:

depositing a composite polymer dielectric film onto a substrate, wherein the composite polymer dielectric film includes a silane-containing adhesion promoter layer formed on the silicon-containing substrate, and a low dielectric constant polymer layer formed on the adhesion promoter layer;

depositing a silane-containing hard mask layer onto the composite polymer dielectric film;

exposing the hard mask layer and the adhesion promoter layer to a free radical-generating energy source to chemically bond the adhesion promoter layer to the underlying silicon-containing substrate and to the low dielectric constant polymer layer, and to chemically bond the composite polymer dielectric film to the hard mask layer;

etching an etched feature in the hard mask layer and the composite polymer dielectric film; and

depositing an electrically conductive material in the etched feature.

2. The method of claim 1, wherein the adhesion promoter layer and the hard mask layer are each formed from at least one material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

3. The method of claim 2, wherein the hard mask layer is formed from an organosilane having a general formula (RZ)-Si-$(W\text{-}T)_3$.

4. The method of claim 1, wherein the adhesion promoter layer and the hard mask layer are each formed from at least one material having a general structure of H_xSi-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

5. The method of claim 1, wherein the low dielectric constant polymer layer is formed from a poly(paraxylylene)-based polymer.

6. The method of claim 1, further comprising forming a silane-containing barrier layer over the hard mask layer, forming a second low dielectric constant polymer layer over the barrier layer, forming a silane-containing etch stop layer over the second low dielectric constant polymer layer, and exposing the barrier layer and the etch stop layer to the free radical-generating energy source to cause the etch stop layer and the barrier layer to chemically bond to the second low dielectric constant polymer layer.

7. The method of claim 6, wherein the etch stop layer is formed from at least one organosilane having a general formula $(RZ)_3$-Si-(W-T), wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group, and wherein a is 0 or an integer.

8. The method of claim 6, further comprising forming a third low dielectric constant polymer layer over the etch stop layer.

9. The method of claim 8, further comprising forming a second hard mask layer over the third low dielectric constant polymer layer.

10. The method of claim 9, wherein exposing the hard mask layer and the adhesion promoter layer to a free radical-generating energy source includes simultaneously exposing

11. The method of claim 10, further comprising:

etching a via through the third low dielectric constant polymer layer, the etch stop layer, and the second low dielectric constant polymer layer;

etching a trench through the third low dielectric constant polymer layer, wherein the trench at least partially overlaps the via; and

depositing an electrically conductive material in the via and the trench.

12. The method of claim 11, further comprising removing electrically conductive material from surfaces adjacent the trench via chemical-mechanical polishing.

13. The method of claim 1, wherein exposing the adhesion promoter layer and the hard mask layer to a free radical-generating energy source includes heating the adhesion promoter layer and the hard mask layer.

14. The method of claim 13, wherein the composite polymer dielectric film and the hard mask layer are heated under a mixture of hydrogen and a noble gas.

15. The method of claim 1, wherein exposing the adhesion promoter layer and the hard mask layer to a free radical-generating energy source includes exposing the adhesion promoter layer and the hard mask layer to a UV light source.

16. A method of forming an electrically conductive element in an integrated circuit, the method comprising:

depositing a polymer dielectric film onto a substrate;

depositing a hard mask layer over the polymer dielectric film;

forming a patterned film of a resist material on the hard mask layer;

etching an etched feature into the composite polymer dielectric layer;

annealing the etched feature in a reducing atmosphere including hydrogen; and

depositing an electrically conductive material in the etched feature.

17. The method of claim 16, wherein the polymer dielectric layer is formed at least partially from a fluorine-containing polymer having a dielectric constant of less than 2.6.

18. The method of claim 16, wherein the polymer dielectric layer is a composite film including a low dielectric constant polymer layer disposed between and chemically bonded to a first organosilane-containing layer and a second organosilane-containing layer.

19. The method of claim 18, wherein the low dielectric constant polymer layer is formed from a poly(paraxylylene)-based polymer.

20. The method of claim 18, wherein the first organosilane-containing layer and the second organosilane-containing layer are formed from at least one material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

21. The method of claim 16, wherein annealing the etched feature in the presence of a reducing atmosphere including hydrogen includes annealing the etched feature at a temperature of between approximately 300 and 400 degrees Celsius.

22. The method of claim 21, wherein annealing the etched feature in the presence of a reducing atmosphere including hydrogen includes annealing the etched feature for a duration of between approximately 2 and 10 minutes.

23. The method of claim 16, wherein annealing the etched feature in the presence of a reducing atmosphere including hydrogen includes annealing the etched feature in a mixture of hydrogen and argon.

24. The method of claim 23, wherein the etched feature is annealed in a mixture of 10% hydrogen in argon.

25. In an integrated circuit, a method of forming an electrical connection to an underlying electrically conductive element, wherein the electrically conductive element is disposed within a first polymer dielectric film, the method comprising:

forming a second polymer dielectric film over the electrically conductive element and the first polymer dielectric film, wherein the second polymer dielectric film has a composite structure including a first silane-containing adhesion promoter layer chemically bonded to a first low dielectric constant polymer layer;

forming an etch stop layer over the second polymer dielectric film;

forming a third polymer dielectric film over the etch stop layer;

forming a hard mask layer over the third polymer dielectric film;

etching a via through the third polymer dielectric film, the etch stop layer, and the second polymer dielectric film to expose the electrically conductive element;

etching a trench through the third polymer dielectric film such that the trench at least partially overlaps the via; and

depositing an electrically conductive material in the via and the trench, wherein the electrically conductive material contacts the electrically conductive element in the first polymer dielectric layer.

26. The method of claim 25, wherein the third polymer dielectric film includes a second silane-containing adhesion promoter layer and a second low dielectric constant polymer layer.

27. The method of claim 25, wherein the etch stop layer is formed from an organosilane material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

28. The method of claim 27, wherein the organosilane material has a general structure of $(RZ)_3$-Si-(W-T).

29. The method of claim 25, wherein the adhesion promoter layer is formed from an organosilane material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

30. The method of claim 25, wherein the hard mask layer is formed from an organosilane material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

31. The method of claim 30, wherein the organosilane material has a general structure of (RZ)-Si-$(W\text{-}T)_3$.

32. The method of claim 25, further comprising exposing the second polymer dielectric film to a free radical-generating energy source to chemically bond the first adhesion promoter layer to the first low dielectric constant polymer layer before depositing the third polymer dielectric layer.

33. The method of claim 32, further comprising exposing the etch stop layer to a free radical-generating energy source to chemically bond the etch stop layer to the first low dielectric constant polymer layer.

34. The method of claim 33, further comprising exposing the third polymer dielectric film to the free radical-generating energy source to chemically bond the third polymer dielectric film to the etch stop layer.

35. The method of claim 34, further comprising exposing the hard mask layer to the free radical-generating energy source to chemically bond the hard mask layer to the third polymer dielectric layer.

36. The method of claim 25, wherein the third polymer dielectric layer includes a second adhesion promoter layer and a second low dielectric constant polymer layer, further comprising exposing the third polymer dielectric layer to a free radical-generating energy course to chemically bond the second adhesion promoter layer to the second low dielectric constant polymer layer.

37. The method of claim 25, further comprising annealing the via and the trench in a reducing atmosphere before depositing the electrically conductive material in the via and the trench.

38. The method of claim 37, wherein the via and the trench are annealed in a mixture of hydrogen in a noble gas.

39. An integrated circuit, comprising:

a substrate;

a first silane-containing layer formed over and chemically bonded to the substrate;

a low dielectric constant polymer layer formed over and chemically bonded to the adhesion promoter layer;

a second silane-containing layer formed over and chemically bonded to the low dielectric constant polymer layer;

an etched feature extending through the second silane-containing layer and at least partially through the low dielectric constant polymer layer; and

an electrically conductive material disposed within the etched feature.

40. The integrated circuit of claim 39, wherein the first silane-containing layer and silane-containing layers are each formed from at least one silane having a general formula of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from the group consisting of -O-, -CH_2-, -$(CH_2)_aC{=}OO$-, and -$(CH_2)_a$-$OO{=}C$-; wherein T is selected from the group consisting of -CR=CR'R", an alkyl halide, and -RC=O; wherein Z is selected from the group consisting of O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4.

41. The integrated circuit of claim 40, wherein the first silane-containing layer is an adhesion promoter layer having a general formula of (RZ)-Si-$(W\text{-}T)_3$.

42. The integrated circuit of claim 40, wherein the second silane-containing layer is a hard mask layer and is formed from a silane having a general formula of (RZ)-Si-$(W\text{-}T)_3$.

43. The integrated circuit of claim 40, wherein the second silane-containing layer is an etch stop layer and is formed from a silane having a general formula of $(RZ)_3$-Si-(W-T).

44. The integrated circuit of claim 39, wherein the low dielectric constant polymer layer is formed from a poly(paraxyxylene)-based polymer.

45. The integrated circuit of claim 39, wherein the electrically conductive material includes copper.

46. The integrated circuit of claim 39, wherein the low dielectric constant polymer layer is a first low dielectric constant polymer layer, further comprising a second low dielectric constant polymer film formed over the second silane-containing layer, and a third silane-containing layer formed over the second polymer dielectric film.

47. The integrated circuit of claim 46, further comprising a third low dielectric constant polymer layer formed over the third silane-containing layer.

48. The integrated circuit of claim 46, wherein the etched feature extends through the third silane-containing layer and the second low dielectric constant polymer layer.

49. The integrated circuit of claim 39, wherein the first silane-containing layer, low dielectric constant polymer layer, second silane-containing layer, etched feature and electrically conductive material are a part of a single Damascene structure.

50. The integrated circuit of claim 39, wherein the first silane-containing layer, low dielectric constant polymer layer, second silane-containing layer, etched feature and electrically conductive material are a part of a dual Damascene structure.